Monolithic Integrated Slot-Blocker for High Datarate Coherent Optical slot switched networks

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***Abstract*— Recent progresses on monolithic SOI-based integration are presented for achieving high performance slot-blocker for cost-sensitive metropolitan and datacenter networks. We review several nodes architectures for such optical slot switching ring networks. Such devices integrate up to 65 functional elements, allowing complex operations such as polarization and wavelength (de)multiplexing with sub-wavelength switching capability. Compact footprint, fast switching time (below 10 ns) as well as high extinction ratio (more than 20 dB) are demonstrated. We demonstrate the fast add/drop operation of advanced modulation formats (56/80 Gbit/s SP-QPSK, 128 Gbit/s PDM-QPSK, 256 Gbit/s PDM-16QAM and 320 Gbit/s PDM-32QAM) using three generations of integrated slot-blockers.**

***Index Terms*— Coherent communications, Integrated optics devices, Silicon Photonics**

I. Towards Coherent Optical Packet Switched Networks

A. Context

Huge traffic growth (up to 560% in 5 years) is expected between 2013 and 2017 in metropolitan optical networks [1]. At the same time, datacenter traffic will increase by 23% on average every year between 2013 and 2018, with 75% of the datacenter-generated traffic remaining within the datacenter [2]. Within some datacenters the growth rate can even reach 100% every year [3]. Today's datacenters are built using Electronic Packet Switching (EPS) leveraging for instance the Ethernet or internet protocol (IP) technologies, which are very energy consuming, and hardly compatible with fine traffic engineering (e.g., on-demand capacity provisioning) needed to tune the datacenter performance. Coherent transmission technologies, which have proved successful in the core segment by drastically decreasing transponder cost per bit per second compared with legacy non-coherent technologies, may soon be needed in the metro and intra-datacenter segments in order to sustain the traffic growth in the latter two segments. Similarly, a second feature of core networks, optical circuit switching (OCS), may also soon appear in datacenters to support long duration, high capacity ("elephant") flows while providing low energy consumption, thanks to the removal of energy-hungry (and costly) opto-electronic conversions at intermediate nodes on the data path, and traffic engineering capabilities; however, OCS, if deployed, will have to co-exist with a finer (e.g., packet) switching granularity technology in order to scale to highly dynamic communication between the hundreds, thousands, or more network switching elements that are customarily deployed in large datacenters [3-4]. Indeed OCS networks are dimensioned for peak demands; when demands are relatively constant with time, as is the case in backbone networks where many demands are aggregated, such provisioning is efficient and wastes little capacity; but OCS is not adapted to networks where many short-lived, time-varying flows compete for the

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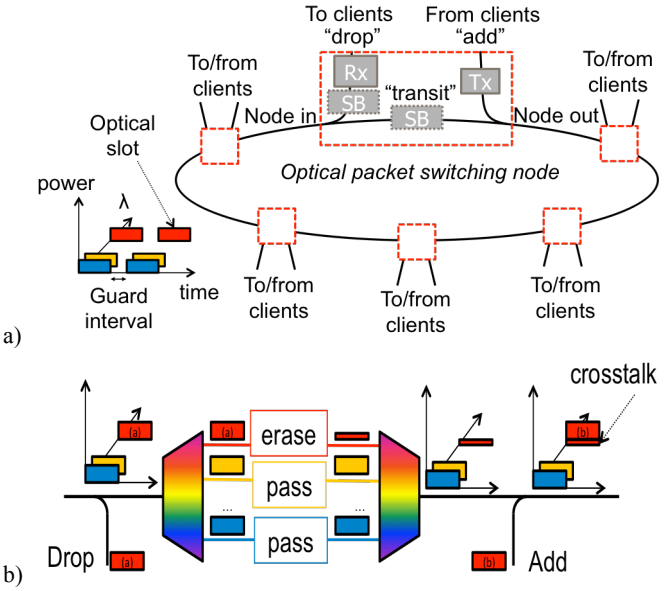


Fig. 1. (a) BOSS ring network (SB : slot-blocker; the part in the dashed box may be integrated using silicon photonics). (b) Typical slot-blocker consisting of a wavelength demultiplexer, one optical gate per wavelength, and a wavelength multiplexer.

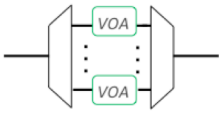
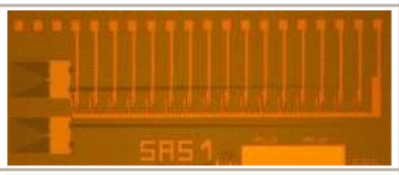
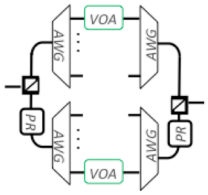
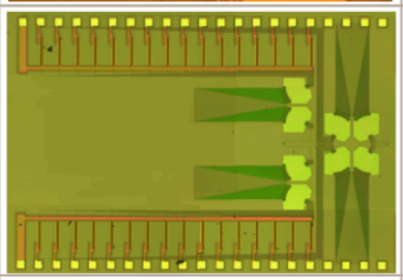
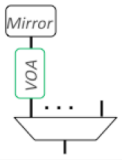
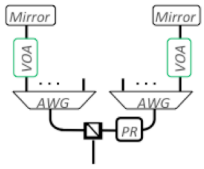
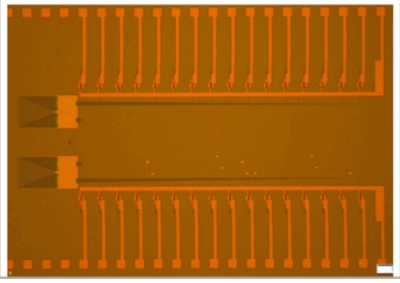
Design	Schematic	Photography	Number of elements	Main characteristics
▪Transmissive ▪Single-polarization [13]			▪AWG: 2 ▪VOA: 16 ▪VG: 2 ▪Total: 18	▪Insertion losses: ~22dB ▪Channel spacing: 200 GHz ▪Maximum attenuation: > 10 dB ▪Switching speed: < 10ns
▪Transmissive ▪Polarization diversity [This work]			▪AWG: 4 ▪VOA: 32 ▪DPVG: 2 ▪Total: 38	▪Insertion losses: ~25dB ▪Channel spacing: 100 GHz ▪Maximum attenuation: > 20 dB ▪Switching speed: < 10ns
▪Reflective ▪Single-polarization [14]			▪AWG: 1 ▪VOA: 16 ▪VG: 1 ▪BGM: 16 ▪Total: 34	▪Insertion losses: ~25dB ▪Channel spacing: 200 GHz ▪Maximum attenuation: > 15 dB ▪Switching speed: < 10ns
▪Reflective ▪Polarization diversity [15]			▪AWG: 2 ▪VOA: 32 ▪DPVG: 1 ▪BGM: 32 ▪Total: 67	▪Insertion losses: ~25dB ▪Channel spacing: 200 GHz ▪Maximum attenuation: > 15 dB ▪Switching speed: < 10ns

Fig. 2. Photographies, schematics, detailed number of elements and main characteristics of the fabricated integrated slot-blockers.

networking resources. For those reasons, optical packet switching (OPS) has been thoroughly investigated in the past two decades (see for instance [5] for a quick review.)

B. Optical packet switching and Burst Optical Slot Switching (BOSS)

Optical packet switching combines the benefits associated with both optical transparency and fast reconfigurability and dynamics; OPS achieves statistical multiplexing hence high network utilization even under highly time-varying traffic demands. Traffic engineering can be made possible through optical packet allocation via an appropriate Software Defined Networks (SDN)-based control plane. With OPS, data is switched at the packet or at least at the sub-wavelength granularity directly in the optical domain, with no electronic conversion or processing. Burst optical slot switching (BOSS) is a version of optical packet switching, where switched entities are slots of the same duration, as shown in Fig. 1(a). Therefore, the combination of coherent and packet switching technologies appears to be an obvious choice to optimize metro and intra-datacenter network performance. Due to the difficulty of implementing multi-degree optical switching fabrics, a number of teams have worked on simpler ring topologies, which can form a mesh through a proper interconnection [6]. Optical packet rings typically relies on the three basic key blocks [5]:

- "Burst-mode" receivers, which are capable of receiving bursts of data (duration: a few microseconds) separated by short guard intervals (duration: well below 1 microsecond).
- Fast wavelength-tunable lasers, which can change their emission wavelength on a per-slot basis, are used as local oscillators to make the coherent receivers fast wavelength-tunable. Fast tunable lasers are also used in the transmitters.
- An optical blocker, implemented either as a static wavelength blocker (e.g., using a wavelength selective switch, WSS), or a dynamic packet blocker that can physically erase slots after they are received so as to reuse the fiber capacity. If the packet blocker is used in a BOSS network, it is commonly called "slot-blocker".

BOSS allows "wavelength reuse," i.e. the capacity used by a slot may be reused by a node in case the slot has been received by this node or an upstream node. Then, the wavelength blocker should be able to block any slot on any wavelength, and it is called a "slot blocker" (SB). In Fig. 1(a), the optical slot switching nodes in the networks typically use a combination of a slot blocker, in the drop or in the transit path, or both, making it one of the key components of optical slot networks.

C. *Slot-blocker integration*

In order to contain cost, several chips can be co-packaged in the optoelectronic transmitter. For example, low cost optical gate as for instance reflective semiconductor optical amplifier (R-SOA) devices could be co-packaged with an arrayed waveguide grating (AWG) [7]. However, monolithic integration is expected to provide larger cost savings than co-packaging and silicon photonics is a promising option providing large-scale integration of photonic components with high-volume manufacturing compatibility. A few silicon photonic devices were proposed as optical gates, such as Mach Zehnder modulator (MZM) [8], ring resonator [9] and variable optical attenuator (VOA) [10]. More complex integration of silicon-based variable optical attenuator (VOA) combined with silica arrayed waveguide grating (AWG) [10] or III-V on silicon semiconductor optical amplifier (SOA) with silicon-on-insulator (SOI)-based AWG [11,12] was proposed in order to build 1xN switching fabrics (with N+1 ports). However, the packaging costs of photonic integrated circuit (PIC) dominate the price of an optoelectronic module, accounting for 60% to 90% of the cost. This is mainly due to the high precision mechanical alignment requirements needed for the optical connections between single mode fibers (SMF) and waveguide components. To overcome cost barriers in PIC module packaging, the obvious solution is to reduce the number of components to be aligned, as proposed with the SB based architecture, which requires 1 or 2 ports only [13-15].

D. *Contributions presented in this paper*

This paper reviews our past work on Silicon Photonics-based slot blockers. . In Section II, we review the design of a slot blocker. In Section III, we study the design of several building blocks used in the slot blocker, such as VOAs, AWGs, vertical grating couplers (VGC) and Bragg grating mirror (BGM), each impacting on the slot blocker optical performance, as demonstrated in Section IV, where several slot blocker implementations are characterized and evaluated in the context or realistic network experiments. In particular, we demonstrate packet-switching and add/drop operation at several data bit rate such as 80 Gbit/s SP-QPSK, 128 Gbit/s PDM-QPSK, 256 Gbit/s PDM-16QAM and 320 Gbit/s PDM-32QAM line rate per channel [13,15].

II. SLOT-BLOCKER IMPLEMENTATION

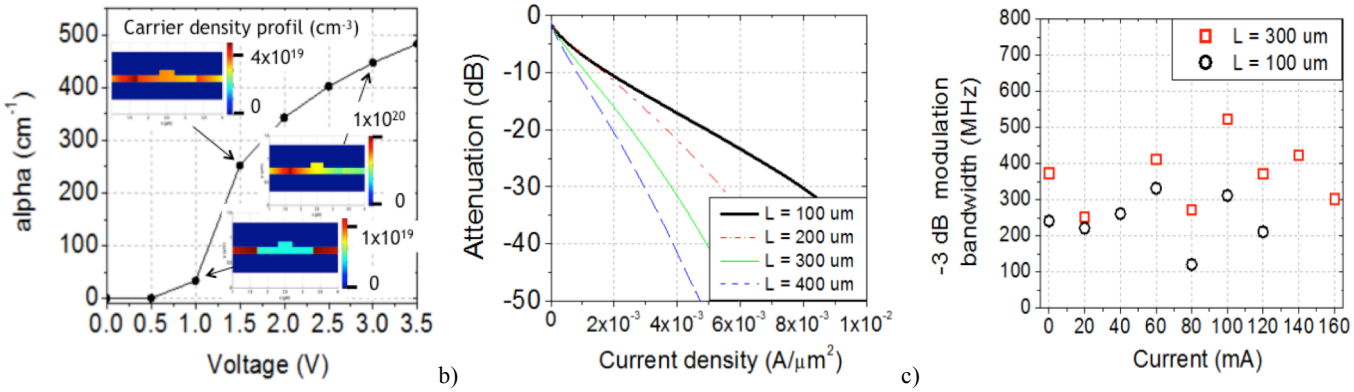
A. *Principle of operation*

A typical slot blocker is shown in Fig. 1(b). The wavelength-multiplexed signal is first demultiplexed, then each wavelength goes through an optical gate, which may block each channel independently based on control signals (not represented in Fig. 1(b)), and finally the wavelengths are multiplexed before exiting the slot blocker. Due to limited switching response of the various optical components used to build BOSS nodes, optical slots must be separated by a "guard interval," during which no data can be transmitted. Overall, the slot length or duration should be chosen to be sufficiently large to make the guard interval negligible, yet sufficiently small to mitigate the impact of packet aggregation on network latency. This in turn means that the guard interval should be kept as small as possible, and hence that the optical gates meant to erase optical slots should be as fast as possible. This is quantified by the gate rise time (the time the gate takes to move from the passing to the blocking state) and conversely the fall time, both of which should be minimized. In addition, optical gates never fully erase light – the remaining part of the "erased" signal combines with added optical signal at the output of the slot blocker, causing degradation of the added signal's quality ("crosstalk"), and possibly rendering its decoding impossible. The ratio (in dB) between the power of a signal before crossing a gate and its power after it is erased is called the extinction ratio (ER). In order to minimize signal quality degradations, and hence maximize the reach (in terms of km or node-count), the optical gate ER should be maximized.

B. *Silicon photonic integration*

1) *Device design*

Fig. 2 shows two possible slot blocker designs: the transmissive (the first two rows) and the reflective architectures (the last two rows). In both cases, we use vertical grating couplers (VGC) in order to couple the light into the PIC. AWGs are used to (de)multiplex the different wavelengths. Two different channel spacing, 200 GHz and



a) b) c)

Fig. 3. (a) Absorption coefficient simulation depending on the bias voltage. (b) Measured attenuation depending of the current density and the length of the VOA. (c) Electro-optics – 3 dB bandwidth depending on the bias current for several VOAs' length. Inset: (a) carrier density profil and (c) SEM picture.

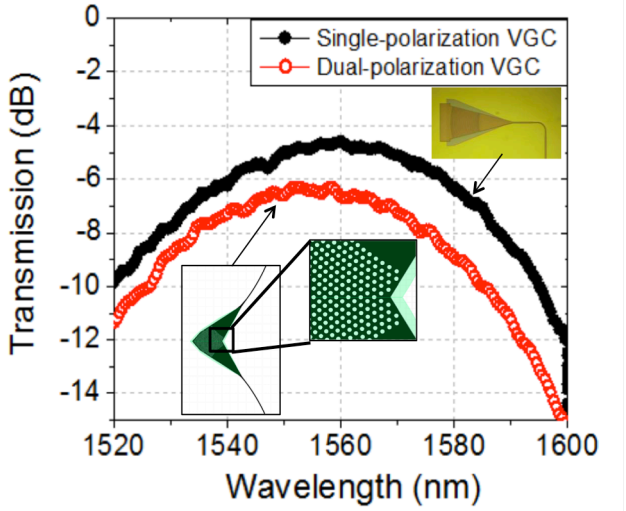


Fig. 4. Transmission of a single-polarization vertical grating coupler and dual-polarization vertical grating coupler.

100 GHz, are proposed. In all configurations, slot/channel blocking is performed by direct modulation of VOAs. One optical gate per wavelength is required. For polarization diversity scheme, light is split/combined at the input/output into two orthogonal polarization components using dual-polarization vertical grating couplers (DPVGC). Each component is aligned with the TE mode of two identical PICs, side-by-side on the same chip. Polarization independent operation can be achieved by synchronously driving both PICs. Please notice that for the transmissive architecture a second AWG (per polarization) is used to re-multiplex the wavelengths before exiting the device through the output port. On the other hand, with the reflective architecture, a Bragg grating mirror (BGM) per wavelength is placed after each VOA in order to reflect back the signals. This way, a single AWG can be used to demultiplex and multiplex the channels, which enter and exit the device through a unique input/output port. Hence, an optical circulator is used to direct incoming optical signals towards the integrated slot blocker, and outgoing selected slots from the device towards following nodes.

2) Fabrication

The chips were fabricated in 220nm overlayer SOI at the CEA-LETI facilities. First, single polarization as well as dual polarization VGC were first patterned using 193 nm deep ultraviolet (DUV) lithography followed by a 70 nm depth Si etching. Then the fabrication of the Si waveguides and the VOA parts were carried out with two self-aligned photolithography steps followed by two Si dry etching steps. The 100nm thick slab of the VOA devices were then N and P doped with different implantations doses before cladding with 1 µm oxide. After silicidation, the AlCu electrodes were formed by DUV lithography and chlorine based reactive-ion etching.

III. Device Characteristics

A. Variable optical attenuator (VOA)

We designed VOAs p-i-n junction, which were forward-biased in order to increase the propagation loss due to the variation of carrier concentration. Free carrier absorption occurs when a material absorbs a photon, and a carrier is excited from an already-excited state to another. We simulated the absorption coefficient, considering a rib waveguide of 220nm thickness and 0.4 um width with an etching of 120 nm of the side. The distance between the edge of the waveguide and the doping zone is considered being 0.6 µm. n and p doping levels are assumed to be $1x10^{19}$ in both cases. The simulated absorption coefficient is displayed in Fig. 3 (a) depending on the bias voltage. The carrier density map is also shown in the inset of the figure and it can be seen by increasing the bias voltage from 1V to 3V, the maximum carrier density inside the p-i-n junction increases from $1x10^{19}$ cm^{-3} up to $1x10^{20}$ cm^{-3}, respectively, therefore increasing the absorption. We show the measured attenuation depending of the device length and the current density ($A/\mu m^2$) on Fig. 3 (b). Attenuation of more than 30 dB is expected for 100 µm-long VOA at $8x10^{-3}$ $A/\mu m^2$. As the VOA length increases, higher attenuation is obtained for constant current density. Therefore longer VOA looks like the most promising candidate however propagation loss as well as the switching speed need to be considered and a trade-off rises between such characteristics. Then a small signal modulation was applied to the VOA in order to determine the electro-optic (E/O) modulation bandwidth. The -3dB E/O bandwidth varied over ~280 MHz range depending on the current and the device length [Fig 3(c)]. The measurement confirms the 10%-90% rise/fall time is less than 10 ns. We compare 100 µm and 300 µm VOA lengths. The E/O bandwidth is similar, a small increase is observed for

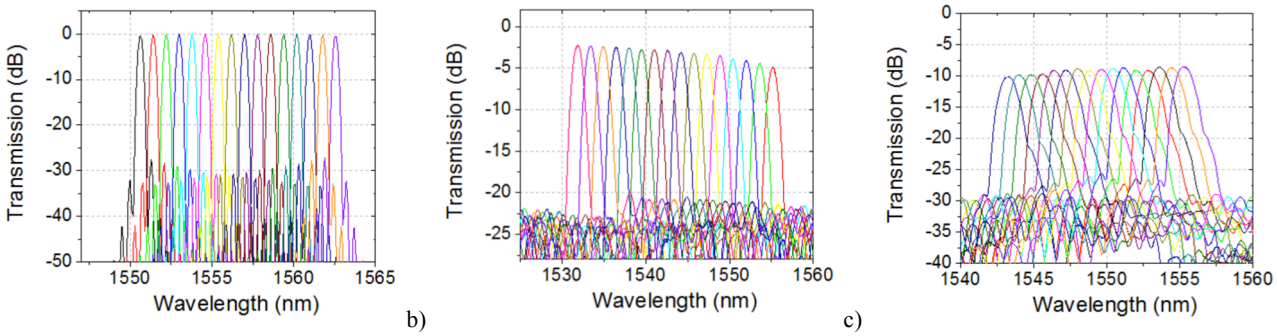


Fig. 5. (a) Simulated AWG transmission for 100 GHz spacing. Measured AWG transmission (b) for 200 GHz spacing and (c) 100 Ghz spacing.

longer device. In the inset of Figs. 3 (c), a SEM picture of a VOA device is shown.

B. *Vertical grating coupler (VGC)*

The two types of VGC were based on the designs performed on the previous FP7 project HELIOS [16] and are now introduced as a building block in the Epixfab process design kit (PDK) of CEA-LETI. In Fig. 4, the performances of a single wire link between two VGCs are reported. The single (respectively dual) polarization coupler for a 10° angle of the fiber exhibited around 5dB (respectively 7dB) of insertion loss.

C. *Arrayed waveguide grating (AWG)*

200-GHz and 100-GHz channel spacing AWGs have been designed and fabricated on SOI wafers with 2-µm thick buried oxide layer (BOX). The smaller sized 200-GHz AWGs can be seen in photographs on the rows number 1, 3 and 4 of Fig. 2, whereas the 100-GHz AWGs are shown on the second row of that same figure. The AWGs were made compact by using small size bends, which are 5-µm radius single mode circular waveguide, all the straight waveguides are multimode waveguides, which allow low propagation loss, since the fundamental mode is further away from the walls of the waveguides. Fig. 5 (a) show simulated normalized transmission for 100-GHz AWG and measured transmission for 200-GHz (Fig. 5 (b)) and 100-GHz (Fig. 5 (c)) AWGs. Both type of AWGs show less than -18dB neighbor channel crosstalk; we can observe lower insertion loss (< -2dB) for 200-GHz AWG than for 100-GHz AWG (<-8dB), due to shorter waveguides; the cross-talk is also better for 200-GHz AWG (>15dB) than for 100-GHz AWG (4-5dB). It should be notice than in a SB, the optical signal goes twice through an AWG making cross-talk a less important issue.

D. *Bragg grating mirror*

As previously explained, reducing the number of fiber alignments results in large cost saving therefore reflective integrated SB are interesting configurations to be investigated. In order to do so, a BGM is placed after each VOA to reflect back the optical signals. 70 nm depth Silicon etching is used to realize the grating on a 220 nm thick waveguide. SEM picture of the top view and the cross section are presented in Fig. 6(a) and (b), respectively. We designed large band BGM in order to cover the full C-band. We use a 290 nm period with a duty cycle of 52%. The length of the BGM is adjusted in order to obtain 100% reflection over more than 100 nm. The reflectivity can be modeled using the transmission matrix method and the reflection coefficient is presented in Fig. 6(c). As we can see, 100% reflection is obtained over ~115nm including the C-band range however in reality, less that 100% reflection is expected due to the scattering and absorption losses as well as the fabrication imperfections.

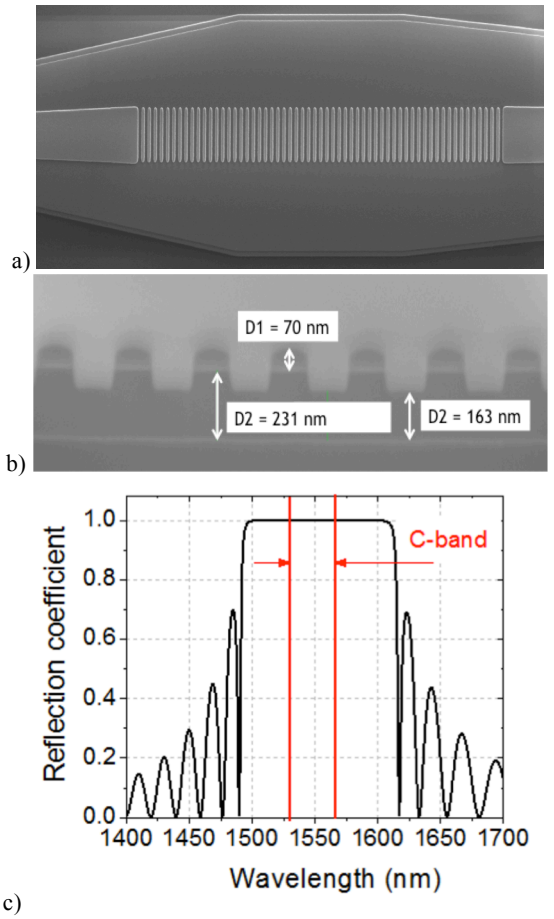


Fig. 6. SEM picture of Bragg grating mirror (a) top view and (b) cross section. (c) Simulated reflection coefficient depending

IV. System Implementation

In this section, we aim to demonstrate the use of the various integrated slot blocker in real network configurations. To do so, we conduct two different experiments. The first one consists of the slot-switching operation at which incoming packets were interleaved with added slots within a BOSS node. We use the slot blocker configuration presented in Fig. 2 (first row [13]). We use two QPSK transmitters (including two tunable lasers) to form continuous flows of either 56 Gb/s or 80 Gb/s packets (28 or 40 Gbaud) with 2 µs duration and 100 ns inter-slot guard bands, for transit and added packets. The packet payloads contained 2^{13}-1 de Bruijn sequences generated with independent primitive polynomials at each transmitter. The transit signal passed through a 50/50 optical coupler and the integrated SB. Any optical packet can thus be transmitted or erased by direct modulation of a silicon-based optical gate. After the SB, the physically emptied time slots were filled with new inserted optical packets at the same wavelength. To do so, one of the QPSK transmitters is used in combination with a commercial SOA, which blocked some of the packets being added. A VOA and a noise loading device were placed before the coherent receiver to adjust the optical signal-to-noise ratio (OSNR) level and the optical power of received signal. Data is then stored for offline processing. Fig. 7 shows the Q^2-factor measurements of a sample channel obtained when varying OSNR (measured in a bandwidth of 0.1 nm) for the output optical packet stream from the BOSS node, when packets stem from the transit or add gates under

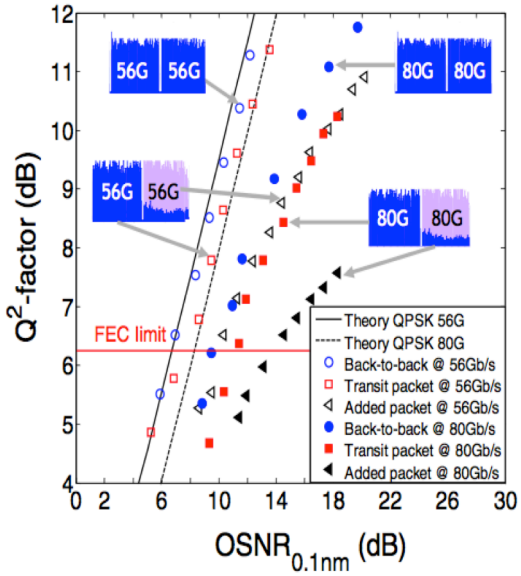
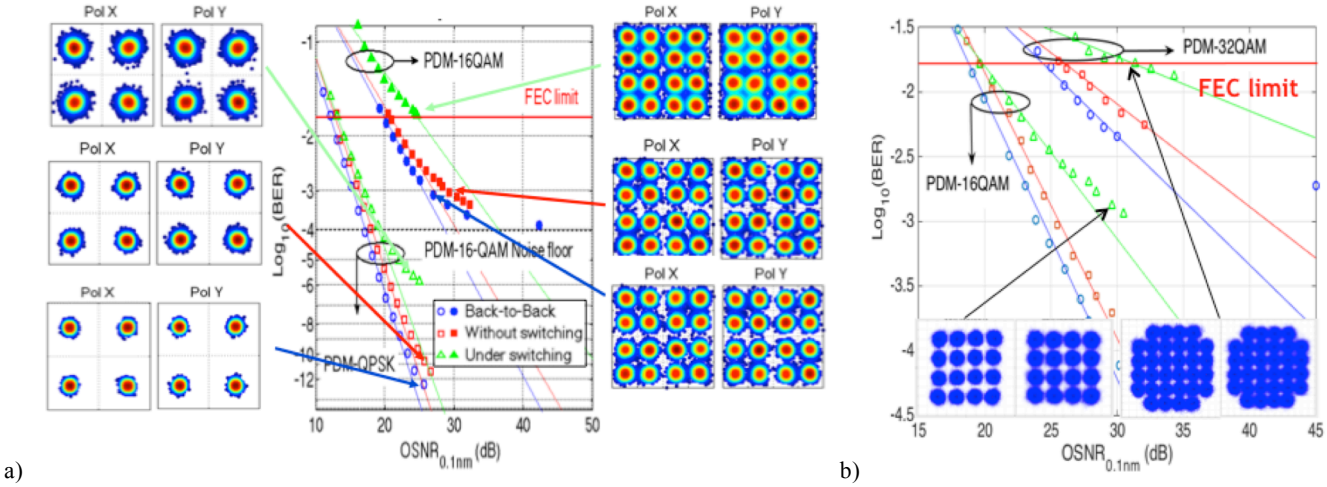


Fig. 7. Q^2-factor measurements considering the transit and the added optical packets at 56 and 80 Gbit/s SP-QPSK using single-polarization transmissive slot-blocker.

switching. For a Q^2-factor of 6.25 dB, corresponding to the soft-decision forward-error-correction (SD-FEC) limit (20% overhead), OSNR sensitivities of 6.7 dB and 9.5 dB were measured respectively for 56 and 80 Gb/s data-rates in back-to-back. Comparing such sensitivities with transit packets, penalties of 0.7 and 1.5 dB were observed at 56 and 80 Gb/s, respectively. On the other hand, for added packets, penalties increased to 3.3 and 4.5 dB at the abovementioned data-rates under switching condition; which was attributed to the limited ER, which causes extra noise on the added packet.

For the second experiment, we use a commercial coherent transponder to generate and detect either PDM-QPSK, PDM-16QAM or PDM-32QAM modulation formats at 128 Gb/s, 256 Gb/s or 320 Gb/s (each at 32 Gbaud that includes 28% overhead for SD-FEC), respectively. The transmitter is (slow) wavelength-tunable and the signal is spectrally shaped with a root-raised-cosine roll-off factor of 0.4. Therefore we use polarization-diversity reflective integrated SB [15]. The real-time bit error ratio (BER) is obtained using such commercial system. Compared to the previous experiment, static add/drop operation is performed as such commercial system is designed for circuit network only. First, the reflective polarization-diversity SB is considered (last row in Fig. 2 [15]). Fig. 8(a) shows the results of the transmission experiment in terms of BER versus the relative OSNR in 0.1 nm for 128 Gb/s PDM-QPSK and 256 Gb/s PDM-16-QAM signals in back-to-back, through or drop/add operations. During drop/add operation we measure the added channel after blocking the dropped channel, thus including in-band crosstalk from the blocked channel. Insets in Fig. 8(a) show six exemplary constellations. In all cases, both polarizations are well recovered confirming the polarization diversity scheme of our device. All PDM-QPSK measurements show performances well below the $1.5\text{x}10^{-2}$ BER limit (SD-FEC threshold). Less than 1-dB OSNR penalty was measured when dropping and adding PDM-QPSK format. In contrast, PDM-16QAM, though providing increased data rate up to 256 Gb/s, is also more sensitive to in-band crosstalk. Under "Through" operation, less than 0.5dB OSNR penalty was measured. However, when dropping and adding a new channel, an OSNR penalty of around 5 dB is observed at the FEC-limit. However the limited ER of this device do not allow switching higher data bit rate.

We then evaluate the integrated SB presented in the second row of Fig. 2 (transmissive configuration [this work]) with higher ER (> 20 dB due to longer VOA). The BER measurements are shown in Fig. 8(b). Under "Through" operation, less than 1 dB OSNR penalty was measured for PDM-16QAM and PDM-32QAM at the SD-FEC limit. When dropping and adding a new channel, no OSNR penalty is observed for 256 Gb/s data-rates compared to back-to-back and less than 6 dB of OSNR penalty is measured for 320 Gb/s data-rates. The PDM-16QAM and PDM-32QAM constellations under switching are shown in the inset of Fig. 8(b). Both polarizations are well recovered however a small mismatch is also observed. Such mismatch is assumed to



a) b)

Fig. 8. Experimental results of BER with respect to the OSNR in Back-to-Back, through and add/drop configurations, (a) 128 Gbit/s PDM-QPSK/256 Gbit/s PDM-16QAM using polarization-diversity reflective slot-blocker and (b) 256 Gbit/s PDM-16QAM/320 Gbit/s PDM-32QAM using the polarization-diversity transmissive slot-blocker.

come from the polarization depend loss (from the dual-polarization grating couplers, the AWGs and the BGMs) of our PIC as well as the polarization dependence of the attenuation on the injected current in the two corresponding VOAs for each polarizations.

V. Conclusion

We demonstrated several integrated silicon-photonics-based slot-blockers. We described the concept, fabrication and system implementation of such technology. The basic building blocks, such as VOA, VGC, AWG and BGM, are investigated and optimized. Then fully integrated slot blockers were fabricated and tested. Different options were considered. First, transmissive single-polarization slot blocker is investigated. 200 GHz-spacing AWG and short VOA are used combined with single-polarization VGC. The device performs wavelength demultiplexing and multiplexing, and high-speed switching (ns timescale). We integrated the SB into a slot-switched network testbed with 56 and 80 Gb/s QPSK optical packets [13]. However, the single polarization and an ER no larger than 10 dB was obtained, limiting the blocking and adding functionality to such 80 Gb/s SP-QPSK channels. With a reflective configuration with only a 1-port package, ER improvement (up to 6 dB) is demonstrated as the optical signal goes back and forth through the VOA [14]. We also designed a dual-polarization slot blocker where polarization independent operation can be achieved by synchronously driving the two PICs. Then we demonstrated an add/drop operation at a record 256 Gb/s line rate per channel for monolithic SOI-based SB using commercial coherent transponders [15]. Finally, we proposed a SB with improved channel spacing (100 GHz) and higher ER. We then demonstrated Add/drop operation of 256 Gbit/s PDM-16QAM and 320 Gbit/s PDM-32QAM signals. All SBs are the small-form factor integrated devices with fast switching capability. The PICs integrate up to 65 functional devices. Such technology is viewed as promising blocks for BOSS network in the metropolitan and datacenters network segments where cost, footprint, flexibility and network efficiency are true concerns.

VI. References

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